THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALAN C. ROGERS

Appeal No. 96-4006
Application 08/300,028[1]

ON BRIEF

Before HAIRSTON, MARTIN, and JERRY SMITH, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

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[1] Application for patent filed September 2, 1994.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 19. In a first Amendment After Final (paper number 7), claims 1, 5 and 13 were amended. In a second Amendment After Final (paper number 15), claims 1, 5, 8, 13 and 17 were amended.[2]

The disclosed invention relates to a phase locked loop clock generator that includes a frequency changer that changes the frequency of a global clock signal while maintaining a reference clock signal and a feedback clock signal at first and second constant frequencies, respectively.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A phase locked loop clock generator comprising:

a phase locking circuit for generating a first clock signal in response to a reference clock signal and a feedback clock signal; and

a frequency changer for generating a global clock signal for said phase locked loop clock generator and said feedback clock signal in response to said first clock signal, said frequency changer changing the frequency of said global clock

[2] According to the examiner (Supplemental Answer, page 2), the latter amendment had the effect of overcoming the indefiniteness rejection of claims 1, 5, 8, 13 and 17.

signal in response to a control signal, with said reference clock signal and feedback clock signal being maintained at a first and second constant frequency, respectively.

The references relied on by the examiner are:

Aldridge	3,898,579	Aug. 5, 1975
Volk et al. (Volk)	4,829,258	May 9, 1989
Hotta et al. (Hotta)	5,133,064	July 21, 1992

Claims 1, 5, 8 and 9 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Volk.

Claims 4 and 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Volk in view of applicant's admitted prior art.

Claims 2, 3, 6, 7, 10, 11 and 13 through 17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Aldridge in view of Hotta.

Claims 18 and 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Volk.

Reference is made to the briefs and the answers for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse all of the rejections.

According to the examiner (Supplemental Answer, pages 3

and 6), Volk discloses a phase locked loop clock generator (Figures 6 and 13) in which the reference clock signal is maintained at a

first constant frequency, and the feedback clock frequency is maintained at a second constant frequency.

Appellant argues (Reply Brief, page 3) that "Volk . . . teaches away from the invention by requiring 'the primary loop to be adjusted . . . by simply adjusting the reference clock frequency' (Col. 10, lines 3-9) (emphasis added). (see applicant's Appeal Brief, pp. 3-4)." We agree. Volk states throughout his disclosure (Abstract; column 2, lines 28 through 30; column 10, lines 3 through 9; and column 11, lines 40 through 42) that the loop frequency characteristics can be programmed by adjusting the reference clock frequency. Thus, the 35 U.S.C. § 102(b) rejection of claims 1, 5, 8 and 9 is reversed because the reference clock is not maintained at a constant frequency.

The 35 U.S.C. § 103 rejection of claims 4 and 12 is reversed because applicant's admitted prior art coupled with Volk neither teaches nor would have suggested to one of ordinary skill in the art keeping the reference clock at a constant frequency.

The 35 U.S.C. § 103 rejection of claims 18 and 19 is reversed because the teachings of Volk would not have

suggested to the skilled artisan a constant reference clock frequency.

Turning to the obviousness rejection of claims 2, 3, 6, 7, 10, 11 and 13 through 17, appellant does not challenge the propriety of modifying the teachings of Aldridge with those of Hotta. Appellant does, however, argue that "the Aldridge feedback loop does not remain synchronous with the Aldridge reference clock signal" (Brief, page 6), and that Hotta allows the "reference signal to lose synchronization with its feedback signal during operation" (Brief, page 7).

Appellant is able to maintain a constant feedback clock signal by using two separate dividers with differently varying divisors. The examiner's contentions (Supplemental Answer, pages 4, 5 and 7) to the contrary notwithstanding, Aldridge's single divider 17 (Figure 1) is incapable of performing such a feat because the divider 17 constantly changes the frequency of the feedback clock signal f_0/n (column 1, lines 24 through 30; and column 3, lines 40 through 44). Hotta discloses a clock generator (Figure 21; column 14, lines 4 through 9) which uses two separate frequency dividers 1304. Hotta does not, however, disclose varying the divisors in the two

dividers. In summary, Hotta, like Aldridge, is incapable of keeping the feedback clock signal at a constant frequency. For this reason, the 35 U.S.C. § 103 rejection of claims 2, 3, 6, 7, 10, 11 and 13 through 17 is reversed.

DECISION

In view of the reversal of all of the rejections, the decision of the examiner is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
JOHN C. MARTIN Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JERRY SMITH Administrative Patent Judge	)	

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James D. Ivey
Law Offices of James D. Ivey
3025 Totterdell Street
Oakland, CA 94611-1742